

Appl. No. 10/605,419  
Amdt. dated January 28, 2005  
Reply to Office action of December 29, 2004

**Amendments to the Claims:**

**Listing of Claims:**

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Claim 1 (original) A flash memory cell structure comprising:

a substrate having a stacked gate;

a select gate formed on the substrate and adjacent to one side of the stacked gate;

10 a first-type doped region located in the substrate and adjacent to the select gate as a drain;

a shallow second-type doped region located underneath the stacked gate and adjacent to the first-type doped region;

15 a deep second-type doped region surrounding the first-type doped region and adjacent to the shallow second-type doped region; and

a doped source region formed on a side of the shallow second-type doped region as a source.

20 Claim 2 (original) The flash memory cell structure of claim 1 wherein a depth of the deep second-type doped region is deeper than a depth of the shallow second-type doped region.

25 Claim 3 (original) The flash memory cell structure of claim 1 wherein the deep second-type doped region has the same doped ions as the shallow second-type doped region.

Claim 4 (original) The flash memory cell structure of claim 3 wherein the

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doped ions of the deep second-type doped region and the shallow second-type doped region are selected from the III A group.

- 5 Claim 5 (original) The flash memory cell structure of claim 1 wherein the doped ions of the first-type doped region and the doped source region are selected from the V A group.

- 10 Claim 6 (original) The flash memory cell structure of claim 1 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited together.

- 15 Claim 7 (original) The flash memory cell structure of claim 6 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited by metal penetrating the junction between the first-type doped region and the deep second-type doped region.

- 20 Claim 8 (original) The flash memory cell structure of claim 6 wherein the first-type doped region and the deep second-type doped region are electrically short-circuited by metal exposed outside the first-type doped region and the deep second-type doped region of the substrate.

- 25 Claim 9 (original) The flash memory cell structure of claim 1 wherein the stacked gate includes a floating gate located over the shallow second-type doped region, and a control gate located over the floating gate.

Claims 10-16 (cancelled)